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10/602,320	06/24/2003	Peter T. Larsen	80107.034US1	1015

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EXAMINER	
PATEL, HETUL B	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,320	LARSEN, PETER T.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 September 2005.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 June 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communication filed on September 22, 2005. Claims 1-28 are again presented for examination.

Information Disclosure Statement

2. The IDS filed on November 05, 2003 has not been received from the Applicant in this Application. Applicant alleges the IDS was filed on November 05, 2003, however, there is no record indicating it is received to US Patent Office.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5 and 6 recite the limitation "repeating the method" in the method claims. This is like an infinite loop in computer programs. It is suggested to replace the phrase "... repeating the method for ..." with "... repeating the issuing, the reading, the programming and the specifying steps for ...".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3-9, 11-12, 19 and 21-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Terauchi (USPN: 5,862,147).

As per claim 1, Terauchi teaches a method of programming a FLASH memory device (i.e. the flash memory 21 in Figs. 1-2) comprising: issuing a blank check command (i.e. blank check operation) to a command register within the FLASH memory device (i.e. the flash memory 21 in Figs. 1-2); reading a status bit (i.e. the bit(s) where the result is written in the second memory area 23 in Fig. 2) in a status register (i.e. the second memory area 23 in Fig. 2) within the FLASH memory device to verify that at least a portion of the FLASH memory device is blank; and programming memory locations within the portion of the FLASH memory device verified as blank (i.e. writing/programming only those addresses that verified as blank, see S41-S44 in Fig. 4) (e.g. see Col. 4, lines 36-58; Col. 5, lines 18-21 and Figs. 1-2 and 4).

As per claim 7, Terauchi teaches a method of blank checking and programming a FLASH memory device (i.e. the flash memory 21 in Figs. 1-2) comprising: receiving a blank check command (i.e. blank check operation) from a device (i.e. the microcomputer 24 in Fig. 2) external to the FLASH memory device; in response to the blank check command received from a device external to the FLASH memory device, reading a plurality of memory locations in at least one block of the memory device; writing to a bit (i.e. the bit(s) where the result is written in the second memory area 23 in Fig. 2) in a status register (i.e. the second memory area 23 in Fig. 2) to indicate whether the at least one block is blank, wherein the status register is accessible by the device external to the FLASH memory device; and receiving data to be programmed in the at least one block (e.g. see Col. 4, lines 36-58; Col. 5, lines 18-21 and Figs. 1-2 and 4).

As per claim 19, see arguments with respect to the rejection of claim 7. Claim 19 is also rejected based on the same rationale as the rejection of the claim 7.

As per claim 3, Terauchi teaches the claimed invention as described above and furthermore, Terauchi teaches that issuing a blank check command comprises: issuing a blank check setup command (i.e. step S42 in Fig. 4); and issuing a blank check confirm command (i.e. step S43 in Fig. 4) (e.g. see Col. 2, lines 36+ and Fig. 4).

As per claims 8, 21 and 27, see arguments with respect to the rejection of claim 3. Claims 8, 21 and 27 are also rejected based on the same rationale as the rejection of the claim 3.

As per claim 4, Terauchi teaches the claimed invention as described above and furthermore, Terauchi teaches that the method further comprising specifying a block

(i.e. the block between the 'RESET' address and 'FULL' address specified) to blank check (e.g. see Fig. 5).

As per claims 5 and 6, Terauchi teaches the claimed invention as described above and furthermore, Terauchi teaches that the method further comprising repeating the listed actions for more than one block in the memory device, i.e. repeating the blank check steps for more than one and each flash memories (blocks) on the wafer (memory device) (e.g. see Fig. 1).

As per claims 22 and 28, see arguments with respect to the rejection of claims 5-6. Claims 22 and 28 are also rejected based on the same rationale as the rejection of the claims 5-6.

As per claim 9, Terauchi teaches the claimed invention as described above and furthermore, Terauchi teaches that reading a plurality of memory locations comprises reading each memory location in the at least one block (i.e. the block between the 'RESET' address and 'FULL' address specified) (e.g. see Col.2, lines 36+ and Fig. 5).

As per claim 11, Terauchi teaches the claimed invention as described above and furthermore, Terauchi teaches that receiving a blank check command comprises receiving an indication of a block to blank check, i.e. receiving the blank check command comprises whether a block is blank or not (e.g. see Col. 4, lines 36-38).

As per claim 12, Terauchi teaches the claimed invention as described above and furthermore, Terauchi teaches that reading a plurality of memory locations comprises reading memory locations (i.e. between the 'RESET' address and 'FULL' address) in

the indicated block (i.e. the block between the 'RESET' address and 'FULL' address specified) (e.g. see Col.2, lines 36+ and Fig. 5).

As per claim 23, Terauchi teaches an electronic system comprising a direct conversion receiver (i.e. the pad 31f in Fig. 3 that receives the test control signals); a processor (i.e. 24 in Fig. 2) coupled to the direct conversion receiver; and a memory device (i.e. 21 in Fig. 2) coupled to the processor, the memory device including a FLASH memory core (i.e. 22 in Fig. 2) and a control block (the combination of 24 and 25 in Fig. 2) adapted to blank check at least a portion of the FLASH memory core; and an external interface (i.e. 61 in Fig. 6) to allow communication between the control block and the processor, wherein the control block is capable of blank checking the at least a portion of the FLASH memory core during a programming operation by the processor (e.g. see Col. 4, lines 36-58; Col. 5, lines 18-21 and Figs. 2-3 and 6).

As per claim 24, Terauchi teaches the claimed invention as described above and furthermore, Terauchi teaches that the control block comprises a microcontroller (i.e. the microcomputer 24 in Fig. 2).

As per claim 25, Terauchi teaches the claimed invention as described above and furthermore, Terauchi teaches that the external interface (i.e. 61 in Fig. 6) comprises a status register (i.e. 23 in Fig. 2) adapted to indicate whether the at least a portion of the memory device is blank (i.e. see Col. 5, lines 18-21; Col. 6, lines 7+ and Figs. 2 and 6).

As per claim 26, Terauchi teaches an electronic system comprising a direct conversion receiver (i.e. the pad 31f in Fig. 3 that receives the test control signals); a FLASH memory device (i.e. 21 in Fig. 2); a processor (i.e. 24 in Fig. 2) coupled to the

direct conversion receiver and the FLASH memory device; and an article having a machine accessible medium (i.e. ROM not shown in the Fig. 2) holding instruction that when accessed result in the processor issuing a blank check command to a command register within the FLASH memory device, reading a status bit in a status register (i.e. the second memory area 23 in Fig. 2) within the FLASH memory device to verify that at least a portion of the FLASH memory device is blank, and programming memory locations within the portion of the FLASH memory device verified as blank (i.e. writing/programming only those addresses that verified as blank, see S41-S44 in Fig. 4) (e.g. see Col. 4, lines 36-58; Col. 5, lines 18-21 and Figs. 2-4).

5. Claims 13-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Shokouhi (USPN: 6,651,199).

As per claim 13, Shokouhi teaches a memory device (i.e. 100 in Figs. 2-3A) comprising: a FLASH memory core (i.e. the memory circuit 120 in Figs. 2-3A); a control block (i.e. 110 in Fig. 2) adapted to blank check at least a portion of the FLASH memory core; and an external interface (i.e. 110 in Fig. 2) to allow communication between the control block and a device (i.e. the JTAG-based operating system) external to the memory device, wherein the control block is capable of blank checking the at least a portion of the FLASH memory core during a programming operation when the memory device is in use in a system (e.g. see Col. 1, lines 36-51 and Figs. 2-3A).

As per claims 14 and 18, Terauchi teaches the claimed invention as described above and furthermore, Terauchi teaches that the external interface comprises a status

register (i.e. 320 in Fig. 4 to hold the current state) adapted to signify that the at least a portion of the FLASH memory core is blank (i.e. VFY state) (e.g. see Col. 7, lines 26-36 and Figs. 4 and 6).

As per claim 15, Terauchi teaches the claimed invention as described above and furthermore, Terauchi teaches that the control block comprises a state machine (i.e. 320 in Fig. 4) (e.g. see Figs. 4 and 6).

As per claim 16, Terauchi teaches the claimed invention as described above and furthermore, Terauchi teaches that the control block comprises a microcontroller (i.e. 220 in Fig. 3A).

As per claim 17, Terauchi teaches the claimed invention as described above and furthermore, Terauchi teaches that the external interface comprising a command register (i.e. 230 in Fig. 3) adapted to receive a blank check command from a device external to the memory device (e.g. see Figs. 2-3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terauchi in view of Salzman (USPN: 5,438,536).

As per claim 2, Terauchi teaches the claimed invention as described above. However, Terauchi does not teach about checking a busy bit. Salzman, on the other hand, teaches that the ready line of the flash memory, which indicates whether the particular flash memory is ready or not, i.e. whether it is busy or not is checked before providing an interrupt signal (e.g. see the abstract and claim 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement step of checking the busy bit in the memory device as taught by Salzman in Terauchi's method. In doing so, the busy bit can be checked before checking the status bit of the memory device to make sure the memory device is not busy; and if the busy bit is indicating busy, then the status bit will not be valid at that time, i.e. it reduces the need for polling status bit of the memory device.

As per claim 20, see arguments with respect to the rejection of claim 2. Claim 20 is also rejected based on the same rationale as the rejection of the claim 2.

As per claim 10, Terauchi teaches the claimed invention as described above. However, Terauchi does not teach about setting a busy bit. Salzman, on the other hand, teaches that the ready line of the flash memory, which indicates whether the particular flash memory is ready or not, i.e. whether it is busy or not is set before providing an interrupt signal (e.g. see the abstract and claim 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement step of checking/setting the busy bit in the memory device as taught by Salzman in Terauchi's method. In doing so, the busy bit can be checked before checking the status bit of the memory device to make sure the memory device is

not busy; and if the busy bit is indicating busy, then the status bit will not be valid at that time, i.e. it reduces the need for polling status bit of the memory device. Salzman also teaches the further limitation of clearing the busy bit (i.e. indicating the ready state) after writing (i.e. after completing the write or erase operation) the bit in the status register (e.g. see claim 1).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MATTHEW D. ANDERSON
PRIMARY EXAMINER